O.P.Code: 19EC0401	R19	H.T.No.									

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
B.Tech I Year II Semester Supplementary Examinations May/June-2024
SWITCHING THEORY AND LOGIC DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 60**

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1		Simplify the following Boolean expression: i) F = (A+B)(A'+C)(B+C). ii)F = A+B+C'+D(E+F)	CO1	L4	12M

OR

2	a	State Duality theorem. List Boolean laws and their Duals.	CO1	L1	6M
	b	Simplify the following Boolean functions to minimum number of literals: i) F = ABC + ABC' + A'B ii) F = (A+B)' (A'+B')	CO1	L4	6M

UNIT-II

3		Minimize the following Boolean function using K-Map F(A, B, C, D)= Σm(0, 2, 4, 6, 8, 10, 12, 14). Realize it using NAND Gates.	CO2	L2	12M

OR

4		Simplify the following Boolean function using Tabulation method Y(A,B,C,D) = Σ(1,3,5,8,9,11,15)	CO2	L4	12M

UNIT-III

5	a	Design & implement BCD to Excess-3 code converter	CO3	L6	6M
	b	Design 32:1 Mux using two 16:1 Muxs and one 2:1 Mux.	CO3	L6	6M

OR

6		Explain Carry Look Ahead Adder circuit with the help of logic diagram.	CO3	L1	12M

UNIT-IV

7	a	Draw the logic symbol, characteristics table and derive characteristics equation of JK flip flop.	CO4	L2	6M
	b	Design T Flip Flop by using JK Flip Flop and draw the timing diagram.	CO4	L6	6M

OR

8	a	Convert S-R flip flop into JK-flip flop. Draw and explain the logic diagram.	CO4	L5	6M
	b	A clocked sequential circuit with single input x and single output z produces an output z=1 whenever the input x compares the sequence 1011 and overlapping is allowed. Obtain the state diagram, state table and design the circuit with D flip-flops.	CO4	L4	6M

UNIT-V

9		Explain the minimization procedure for determining the set of equivalent state of a specified machine M.	CO5	L1	12M

OR

10		Give the logic implementation of a 32x4 bit ROM using a decoder of a suitable figure.	CO5	L6	12M

***** END *****